REMARKS

The Office Action of February 21, 2006 was received and reviewed. The Examiner is thanked for reviewing this application.

Claims 1-5 are pending for consideration, of which claim 1 is independent.

Referring now to the detailed Office Action, claims 1-5 stand rejected under 35 U.S.C. §112, 2nd paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The Examiner cited a number of limitations in the claims that lack proper antecedent basis. In response, Applicant has amended claims 1-5, as shown above.

Claims 1-5 stand rejected under 35 U.S.C. §102(b) as anticipated by Li et al. (U.S. Patent No. 5,974,245 – hereafter Li). Further, claims 1, 3, and 5 stand rejected under 35 U.S.C. §102(e) as anticipated by Tetelbaum (U.S. Patent Publication No. 2005/0050497 – hereafter Tetelbaum). These rejections are respectfully traversed at least for the reasons provided below.

In the rejection of claims 1-5 over Li, the Examiner asserted that Li teaches Applicant's claimed step of determining the number of clocks different in delay amount. The Examiner cited Fig. 3 of Li as disclosing the step of determining the number of clocks. However, col. 3, line 62 of Li describes Fig. 3 as a diagram of a netlist containing clock nets. Applicant respectfully asserts the Fig. 3 and the specification of Li does not teach, disclose or suggest the step of determining the number of clocks different in delay amount as recited in Applicant's claim 1. Rather, Li teaches a method and apparatus for determining parameters for subtrees of a clock trees and inserting buffers into the subtrees based on the subtree parameters. Page 4, second paragraph of the present specification and the Abstract of the Disclosure discuss known technique of inserting buffer blocks in signal paths to change signal delay value that appears similar to Li's method. The specification of the present invention also discusses the problems with inserting buffer blocks in signal paths to effect signal delays.

The Examiner further asserts that col. 1, lines 50-53 and Figs. 3, 9 and 11 of Li as disclosing Applicant's second step for allocating clocks supplied to respective circuits. However, Applicant cannot find any disclosure in Li supporting the Examiner's assertion. As noted above, Fig. 3 of Li is a diagram of a netlist containing clock nets. Fig. 9 is a flow chart

describing steps for moving buffers to their closest legal location, Fig. 10 is a flowchart describing steps for verifying that the buffered clock tree satisfies circuit requirement, and Fig. 11 is a flowchart describing steps for computing pin-to-pin delay, according to col. 4, lines 16-23 of Li. Applicant respectfully asserts that the portions of Li cited by the Examiner completely fails to disclose Applicant's second step of allocating clocks supplied to respective circuit.

Further, Applicant respectfully submits that claim 1 of the present invention recites a number of steps taken in a sequence that constitutes a process. The steps of Li alleged as equivalent to Applicant's claimed steps do not follow the sequential order as Applicants' claimed steps. That is, the Examiner selected various features of Li that are not relevant to Applicant's claimed steps and mischaracterized as equivalent to Applicant's claimed steps.

As mentioned above, Applicant's invention is different from Li and there is no steps claimed in Applicant's invention that relates to a method of Li for making an integrated circuit by inserting buffers into a netlist.

Further, the invention of Li can be seen in a high-level flow diagram Fig. 4. In contrast with Li, Applicant's invention, as recited in claim 1, relates to determining the number of clocks different in delay amount, determining delays in the clocks on the basis of pres-set conditions for constraint timings, allocating clocks to respective circuits, optimizing timings to meet timing constraint condition, determining whether results of analyses of the respective timings correspond to violation of the constraints of timings, and repeating the above steps until timing optimization is achieved for the respective circuits.

The Examiner is invited to review at least, e.g., Figs. 3 and 5, and their respective disclosure in the specification for support for the features of claim 1. Fig. 1, particularly reference numeral 26 denoting a circuit design functional unit and reference numeral 30 denoting a clock generating functional part, also supports the features of claim 1.

Applicant's invention as recited in claim 2 further includes the layout design functional unit (block 28 of Fig. 1) that follows sequentially the above-mentioned circuit design functional unit (block 26 of Fig. 1 and a high-level diagram in Fig. 2) of claim 1. Fig. 4 shows the layout design routine performed in block 28 of Fig. 1. The steps of claim 2 are directed to the layout design routine in Fig. 2 and Fig. 4.

Although Li teaches minimizing clock skew, as the design of integrate circuit is often involves minimizing clock skew, Li does not teach the steps of claim 1 and the step of

adjusting skews for each of the clocks in combination with other steps of claim 2.

In the interest of keeping history compact, the arguments set forth in relation to claim 1 are also applicable to the rejection of dependent claims 2-5 with respect to Li.

With respect to Tetelbaum, although the Examiner asserted that Applicant's claimed steps are disclosed in Tetelbaum, Applicant cannot find any evidence supporting the Examiner's assertion. In supporting the rejection of claim 1, for example, the Examiner cited various numerous parts of Tetelbaum that are out of context and order. If the Examiner maintains the rejection over Tetelbaum, Applicant would respectfully request the Examiner to show at least a flow diagram and provide a comparison of the features in the flow diagram allegedly anticipating Applicant's claimed feature. As is, the rejection relies on a number of figures and text of Tetelbaum that are incoherent, and the rejection of each claim based on Tetelbaum is broad and ambiguous as to which particular feature the Examiner is asserting as equivalent to Applicant's claimed features.

Applicant respectfully asserts that Tetelbaum discloses a method of cell placement and clock tree synthesis including the steps of (a) identifying critical paths in an integrated circuit design; (b) partitioning the integrated circuit design into a timing group for each of the critical paths; (c) assigning each flip-flop in a critical path to a timing group corresponding to the critical path; (d) performing a cell placement to minimize a function of propagation delay and maximum distance between flip-flops within each timing group; and (e) constructing a clock sub-net for each timing group, as shown in paragraph [0005]. The remaining of the disclosure of Tetelbaum discuss in details steps (a)-(e). As can be seen in the steps of Tetelbaum above, Tetelbaum completely fails to disclose at least Applicant's first step for determining the number of clocks different in delay amount and determining delays in the clocks on the basis of pre-set conditions for constraint of timings. Should the Examiner maintains this rejection, Applicant would request the Examienr to point out which of the steps (a)-(e) of Tetelbaum is equivalent to Applicant's first step, for example.

Consequently, since each and every feature of the present claims is not taught (and is not inherent) in the teachings of Li and Tetelbaum, as is required by MPEP Chapter 2131 in order to establish anticipation, the rejection of claims 1-5, under 35 U.S.C. §102(b) and (e), as anticipated by Li and Tetelbaum is improper.

In view of the arguments and amendments set forth above, Applicant respectfully requests reconsideration and withdrawal of the pending rejections, and that the application be passed to issue. If a conference would expedite prosecution of the instant application, the Examiner is hereby invited to telephone the undersigned to arrange such a conference.

Respectfully submitted,

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